Astrophysics Research And Analysis

Driver ASIC environmental testing and performance optimization for space-based active mirrors



Completed Technology Project (2018 - 2020)

Project Introduction

Direct imaging of Earth-like planets requires techniques for light suppression, such as coronagraphs or nulling interferometers, in which deformable mirrors (DM) are a principal component. On ground-based systems, DMs are used to correct for turbulence in the Earth's atmosphere in addition to static aberrations in the optics. For space-based observations, DMs are used to correct for static and quasi- static aberrations in the optical train. State-ofthe-art, high-actuator count deformable mirrors suffer from external heavy and bulky electronics in which electrical connections are made through thousands of wires. We are instead developing Application Specific Integrated Circuits (ASICs) capable of direct integration with the DM in a single small package. This integrated ASIC-DM is ideal for space missions, where it offers significant reduction in mass, power and complexity, and performance compatible with high-contrast observations of exoplanets. We have successfully prototyped and tested a 32x32 format Switch-Mode (SM) ASIC which consumes only ~2mW static power (total, not per-actuator). A number of constraints were imposed on key parameters of this ASIC design, including sub-picoamp levels of leakage across turned-off switches and from switch-tosubstrate, control resolution of ~0.04 mV, satisfactory rise/fall times, and a near-zero on-chip crosstalk over a useful range of operating temperatures. This driver ASIC technology is currently at TRL 4. This Supporting Technology proposal will further develop the ASIC technology to TRL 5 by carrying on environmental tests and further optimizing performance, with the end goal of making ASICs suitable for space-based deployment. The effort will be led by JPL, which has considerable expertise with DMs used in high-contrast imaging systems for exoplanet missions and in adaptive optic systems, and in design of DM driver electronics. Microscale, which developed the prototype of the ASIC-DM, will continue its development. We propose a three-part program to advance the device maturity. The effort will cover (1) radiation hardness, (2) thermal-vacuum environment tests, and (3) parameter performance optimization. We expect to implement the results in an optimized ASIC design for NASA's space applications, expanding the current state-of-the-art into radiation-hardened electronics robust enough for a space environment. This effort will fill technology gaps listed in the Exoplanet Exploration Program Technology Plan 2017: "The challenge is believed to not be the mosaicking of 48×48 devices or 32×32 devices (to reach 128×128) but rather dealing with the enormous number of interconnects and their electronics.". After the close of this effort, continued ASIC development is of course planned, leading to further improvement in parameters



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Organizational Responsibility

Responsible Mission Directorate:

Science Mission Directorate (SMD)

Lead Organization:

California Institute of Technology (CalTech)

Responsible Program:

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Primary U.S. Work Locations and Key Partners



Organizations Performing Work	Role	Туре	Location
California Institute of Technology(CalTech)	Lead Organization	Academia	Pasadena, California
Jet Propulsion Laboratory(JPL)	Supporting Organization	NASA Center	Pasadena, California
Microscale, Inc.	Supporting Organization	Industry Small Disadvantaged Business (SDB)	Woburn, Massachusetts

Primary U.S. Work Locations	
California	Massachusetts

Project Management

Program Director:

Michael A Garcia

Program Manager:

Dominic J Benford

Principal Investigator:

Camilo A Mejia

Co-Investigators:

Karen R Piggee Lewis C Roberts Jean C Shelton Yuqian Wu Xingtao Wu

Technology Areas

Primary:

- TX02 Flight Computing and Avionics
 - └─ TX02.1 Avionics
 Component Technologies
 └─ TX02.1.6 Radiation
 Hardened ASIC
 Technologies

Target Destination

Outside the Solar System